CLAIMS:

1. Detection means for detecting information in a signal (s), comprising integration means (INT) for integrating the signal (s) over time, such that the integration means (INT) is periodically reset at about the start time reference (T_B) of a periodic time interval (T_i); and a sample&hold circuit (SH) for periodically sampling and holding the integrated signal (int) at about an end time reference (T_E) of the periodic time interval (T_i) and thereby delivering a further signal (fs), characterized in that the detection means comprises a chain (CHDL) of signal time delay elements, an input of the chain (CHDL) being coupled to receive the further signal (fs); and combining means (CBMNS) having combining inputs coupled to signal taps of the chain (CHDL), the number of the combining inputs and the positions of coupling of the combining inputs to the signal taps of the chain (CHDL) corresponding to the information in the signal (s).

2. Detection means as claimed in claim 1, characterized in that the information comprises a bit synchronization part followed by a word synchronization part or followed by one of a plurality of possible types of data bit parts, and in that the combining means (CBMNS) delivers a combining output signal corresponding to the bit synchronization part followed by a word synchronization part and delivers combining output signals for each bit synchronization part followed by a possible type of data bit part.

3. Detection means as claimed in claim 2, characterized in that the detection means comprises processing means (PRMNS) for processing all the combining output signals, the processing is accomplished such that, during a predetermined number of the time intervals (T_i), in each time interval (T_i) the lowest (highest) signal value of the signal values of all the combining output signals is detected together with an accompanying position number corresponding to the corresponding time interval (T_i), and that the position number corresponding to the lowest (highest) detected signal value within the predetermined number of time intervals (T_i) is deemed to be the correct position (P_0) of the bit synchronization part followed by a word synchronization part.

4. Detection means as claimed in claim 3, characterized in that the detection means comprises further processing means (FPRMNS) for further processing the deemed correct positions (P_0) delivered by the processing means (PRMNS) of the bit synchronization part followed by a word synchronization part, the further processing means (FPRMNS) examining the positions of the deemed correct positions (P_0) of the bit synchronization part followed by a word synchronization part during a substantially longer period of time as compared with the predetermined number of time intervals (T_i), the further processing means (FPRMNS) comprising an up/down counter (CNT) having a registered value (RCN) which is incremented (decremented) by a unit value up to a predetermined reference value (PRV) of the up/down counter (CNT), whenever a deemed correct position (P_0) of the bit synchronization part followed by a word synchronization part occurs at the position expected by the further processing means (FPRMNS), and which registered value (RCN) is decremented (incremented) by a unit value whenever a deemed correct position (P_0) of the bit synchronization part followed by a word synchronization part does not occur at the position expected by the further processing means (FPRMNS), the further processing means (FPRMNS) delivering positions (P_1) of the bit synchronization part followed by a word synchronization part with improved position reliability accomplished by the manner of operation of the further processing means (FPRMNS) in which the position (P_1) of the bit synchronization part followed by a word synchronization part which is delivered by the further processing means (FPRMNS) is equal to the position expected by the further processing means (FPRMNS) as long as the registered value (RCN) is above (below) a further predetermined reference value (FPRV), and in which the position (P_1) of the bit synchronization part followed by a word synchronization part which is delivered by the further processing means (FPRMNS) is equal to the position (P_0) delivered by the processing means (PRMNS) when the registered value (RCN) becomes equal to the further predetermined reference value (FPRV), in which latter case the up/down counter (CNT) is reset.

5. An apparatus for at least reading data from a disk (1) with address data (2) available on said disk (1), comprising means for deriving a signal (s) during reading of the disk (1), which signal (s) is a representation of the address data (2), and comprising detection means as defined in one of the preceding claims.

6. An optical disk drive for at least reading data from an optical disk (1) with address data (2) available in a pre-groove (4) of said optical disk (1), comprising means for deriving a signal (s) during reading of the optical disk (1), which signal (s) is a representation of the address data (2), and comprising detection means as defined in claim 1, 2, 3, or 4.

7. A magneto-optical disk drive for at least reading data from a magneto-optical disk (1) with address data (2) available in a pre-groove (4) of said magneto-optical disk (1), comprising means for deriving a signal (s) during reading of the magneto-optical disk (1), which signal (s) is a representation of the address data (2), and comprising detection means as defined in claim 1, 2, 3, or 4.

8. A method of detecting address data (2) in a signal (s), comprising the steps of:
- periodically integrating the signal (s) over time during a time interval (T_i),
- sampling and holding the integrated signal (int) at about the end (T_B) of each time interval (T_i) and thereby delivering a further signal (fs),
- delaying the further signal (fs) and thereby providing a plurality of delayed signals having various delays,
- combining at least part of the delayed signals in a manner which corresponds to the address data (2) in the signal (s).

9. A method of detecting address data (2) in a signal (s), which address data (2) comprises a bit synchronization part followed by a word synchronization part or followed by one of a plurality of possible types of data bit parts, the method comprising the steps of:
- periodically integrating the signal (s) over time during a time interval (T_i),
- sampling and holding the integrated signal (int) at about the end (T_B) of each time interval (T_i) and thereby delivering a further signal (fs),
- delaying the further signal and thereby providing a plurality of delayed signals having various delays,
- combining at least part of the delayed signals in a manner which corresponds to the address data (2) in the signal (s), and thereby delivering a combining output signal corresponding to the bit synchronization part followed by a word synchronization part, and thereby delivering combining output signals for each bit synchronization part followed by a possible type of data bit part.

10. A method as claimed in claim 9, characterized in that the method further comprises the step of processing all the combining output signals such that, during a predetermined number of the time intervals (T_i), in each time interval (T_i) the lowest (highest) signal value of the signal values of all the combining output signals is detected together with an accompanying position number corresponding to the associated time interval (T_i), and that the position number corresponding to the lowest (highest) detected signal value within the predetermined number of time intervals (T_i) is deemed to be the correct position (P_0) of the bit synchronization part followed by a word synchronization part.

11. Detection means for detecting information in a signal (fs), comprising a chain (CHDL) of signal time delay elements, an input of the chain (CHDL) being coupled to receive the signal (fs); and combining means (CBMNS) having combining inputs coupled to signal taps of the chain (CHDL), the number of the combining inputs and the positions of coupling of the combining inputs to the signal taps of the chain (CHDL) corresponding to the information in the signal (fs).